RESEARCH ARTICLE OPEN ACCESS

Testing DRAM and Correcting errorsby using Adaptive Technique

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Abstract
DRAM(dynamic random access memory) is most widely used in memorytoday. Leakage power is the main issue of DRAM cell. Iteffects the performance of the DRAM. In this paper introduce a new technique ie adaptive technique a spare wire is used to reroute the data in cell which is damaged

I. INTRODUCTION

VLSI (very large scale integration) is the process of integrating number of transistor into a single chip. The size of transistor is one of major issue in early days, idea of integrating components on a single silicon wafer came to existence led to development in small scale integration(SSI) in early 1960s,then medium scale integration(MSI) in late 1960s and large scale integration and VLSI came to existence in 1970s and 1980s.

DRAM(dynamic random access memory) is most widely used in memory today. DRAM stores each bit of data in capacitor. The charge on the capacitor indicates logic'1' and absence of charge in capacitor indicates logic'0'.These DRAM is tested by manufactures in order to determine their quality and the price of DRAM is determined by the sequence of the test. Now the size of DRAM decreases because of growth of modern technology. The ITRS reports that the minimum feature size of DRAM will be 20nm in 2017 and 2023 it will be 10nm.

The main memory of personal computer is DRAM and it is used in laptops videogames tablets etc.There are two different types of RAM. Static RAM and dynamic RAM.DRAM has high density because it require one transistor and a capacitor bit of data instead of SRAM it require 4 or 6 transistors. There are 2 lines word line and bitline.To improve the performance,speed and write -read capabilities the DRAM memory may be split into small sub array. It will shorten the time to access the individual cell

This paper is organized as follows. Section II Basic Operation Section III Architecture of DRAM.Section IV Basic concepts.Section V Testing DRAM.Section VI Modification. Section VII Simulation Result.

II. BASIC OPERATION

When the voltage is applied to the gate of the access transistor through the word line the access transistor will turn on and the value on the bitline which is transfer to the capacitor. The capacitor will retain that value for limited period ie until the access transistor is turn off. Due to the leakage the stored value in capacitor gradually dissipates. Before the data dissipate refresh operation must be performed ie periodically read out and written back process. Otherwise the value stored in capacitor will no longer resolvable.

III. ARCHITECTURE OF DRAM

DRAM is a rectangular array of memory cells which is used for the read and write operations.FIG 1-the bit lines are connected to the sense amplifier and the word lines are connected to the row decoder[1].There are different types of cell array noises

1.WL to BL coupling noise 2.BL to BL coupling noise

The WL to BL coupling noise is reduced by using folded bit line array. Here bitlines are connected parallel to the sense amplifier .This architecture is called folded bit line array. its feature size is 8F2.There is another type of architecture called as open bit line array and its feature size is 6F2 or 4F2.There is no difference in operation of folded bit array and open bit array.The folded bit array is used in this paper.BL to BL coupling noise is dramatically increase because of the size of dram decrease as part of the integration. Apart from the coupling noises there are another problems like leakage currents. The sub threshold leakage current increase exponentially when size of DRAM decrease

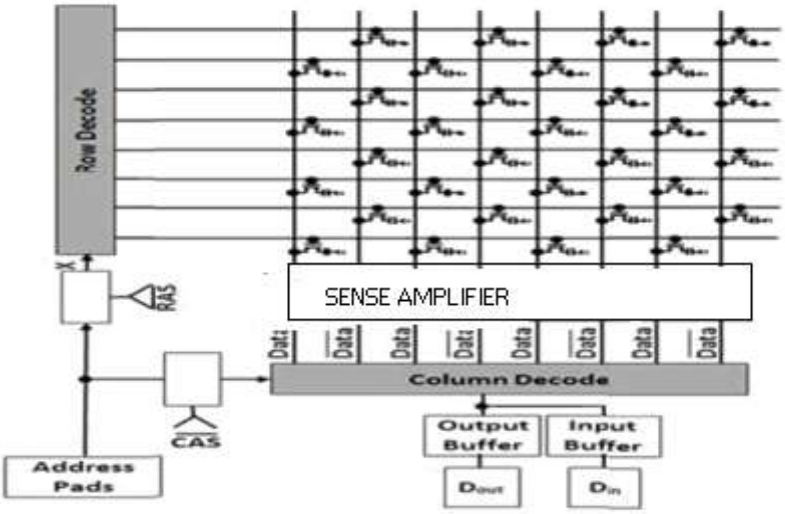


Fig1:DRAM architecture

IV. BASIC CONCEPT

During the read operation of the first word line , the data stored as '1' is transferred to the bitline through the gate transistor. Then bit line is pulled up to 1 and bit bar line pulled down to '0' by the sense amplifier. The first word line is activated at particular time, the bit line cells stored as '0' are stressed during that period because of the voltage difference between the cell data and the bitline.The stress of the cell stored as same voltage level of the bit line are ignored. The cell stored as '1' data at bit bar line are also stressed by voltage difference between bitbarline and cell. If the cell have a defect due to threshold leakage current the defect cell changed to opposite value during the stress time. By setting appropriate test time we can screen the defect cells.

V. TESTING DRAM

In this paper compare faulty DRAM with faultless DRAM using XOR gate. if output of is 1 so we can identify it is faulty, otherwise it is faultless.

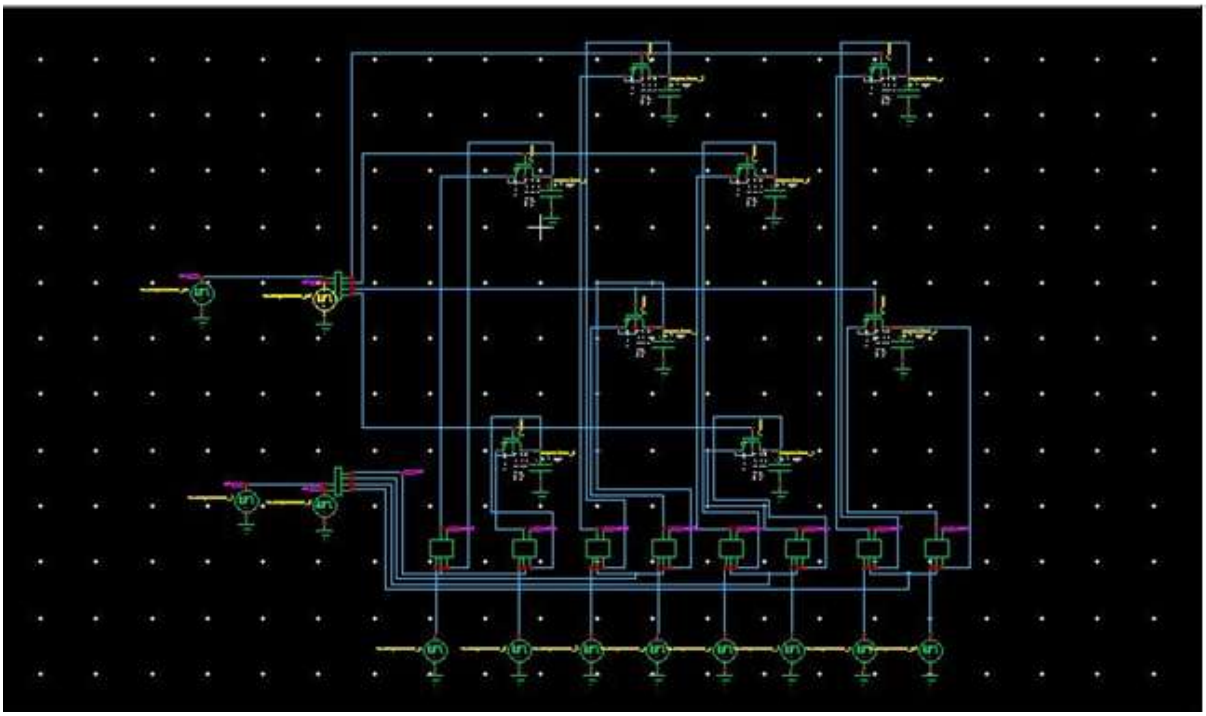
VI. MODIFICATION

If permanent error is detected in order to maintain coding strength spare wire is used .it will not interrupt the data flow. In this method if one transistor is damaged, so unable to store any one bitof data. If we detect the error in DRAM using different test but unable to correct .so we simply need to throw away that DRAM. in order to avoid that circumstances we reroute the data through a spare wire. so if one transistor failed we doesn't need to remove the whole DRAM.

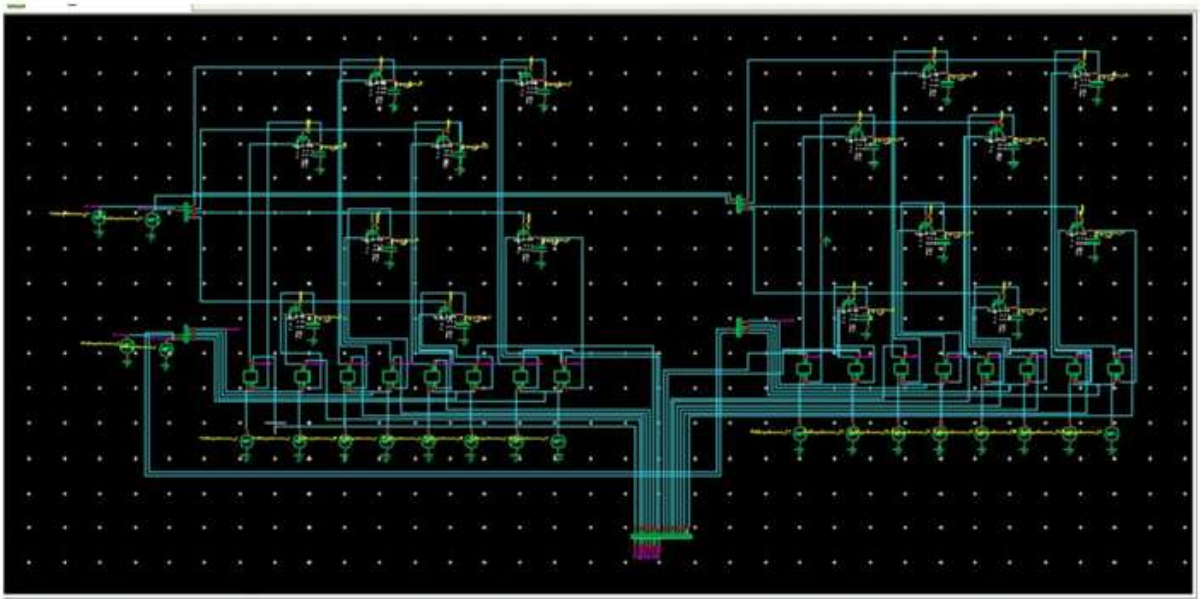
In DRAM sense amplifier is used to get the data from each transistor. instead of using sense amplifier, coupled sense amplifier will improve the performance of DRAM with minimum leakage.

VII. SIMULATION RESULTS

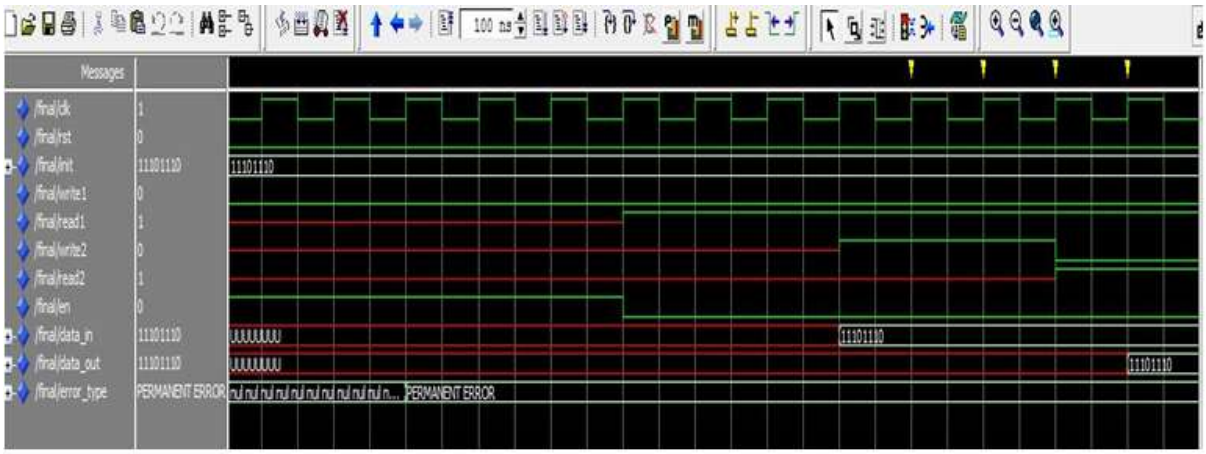
1) Basic DRAM cell



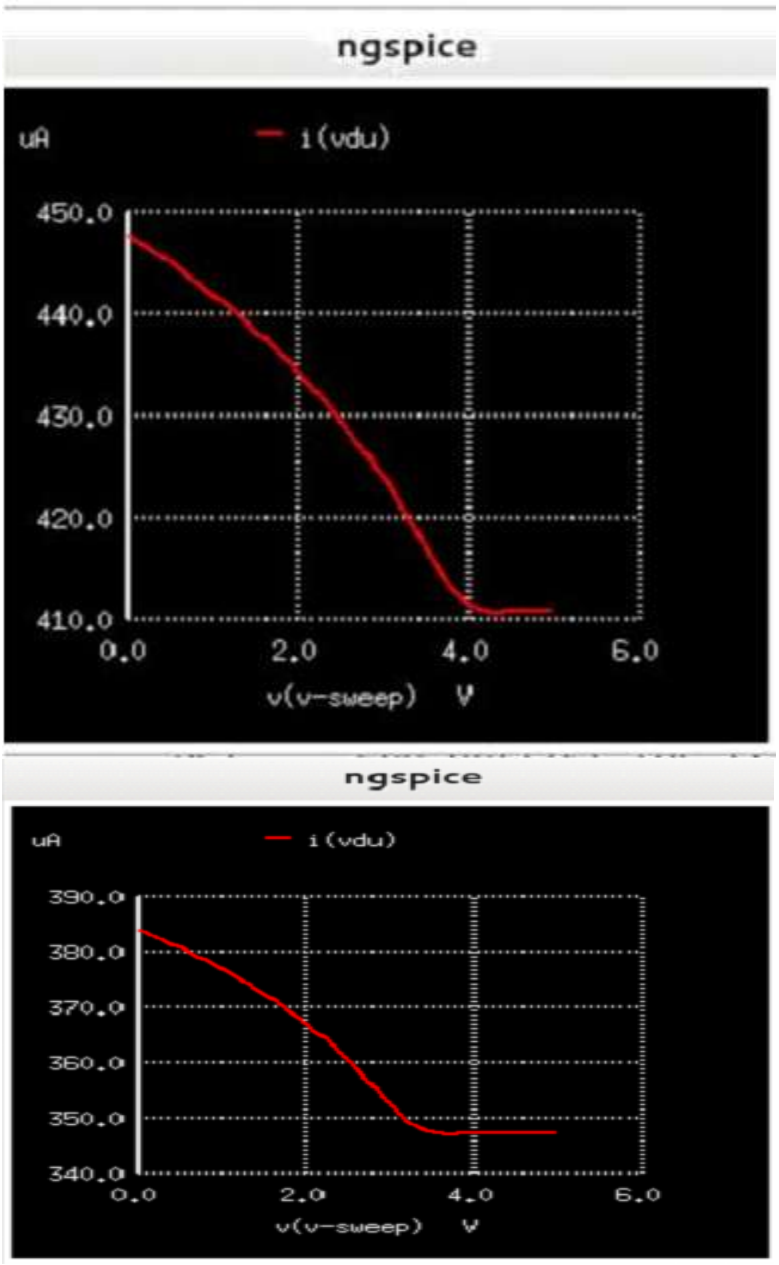
2)Testing the DRAM using XOR gate



3)Adaptive technique



Sense amplifier and Coupled sense amplifier (Leakage Current)



VIII. Conclusion

DRAM is commonly used in memory today.in this paper explained that if any error is detected by the test it can able to correct by using the adaptive technique ie using spare wire and instead of using sense amplifier coupled sense amplifier reduce the leakage current in the dram cell.

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